

Attorney's Docket No.: 06618-917001 / CIT3325-C1P

Amendment to the Claims:

This listing of claims replaces all prior versions, and listings, of claims in the application:

1. (Original) A method, comprising:

preparing a carrier wafer to have a support wafer made of a semiconductor material, a carrier passivation layer formed on a surface of the support wafer, and a membrane formed on the carrier passivation layer, wherein the carrier passivation layer is inert to a gaseous etchant that etches the semiconductor material;

patterning a surface of a device wafer made from the semiconductor material to form a plurality of posts, each post having a top flat surface;

forming a passivation layer on exterior surfaces of the device wafer without covering each top flat surface of each post;

placing the carrier wafer on the device wafer to have the membrane directly contact top flat surfaces of the posts;

forming a direct semiconductor-to-semiconductor bonding between the membrane and the top flat surfaces to bond the carrier wafer to the device wafer;

exposing the bonded carrier wafer and the device wafer to the gaseous etchant to etch away the support wafer in the carrier wafer and to expose the carrier passivation layer; and

removing the carrier passivation layer to transfer the membrane to the device wafer.

2. (Original) The method as in claim 1, wherein the support wafer is made of silicon and the gaseous etchant is XeF_2 .

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3. (Original) The method as in claim 2, wherein the carrier passivation layer in the carrier wafer and the passivation layer on the device wafer are silicon oxide.

4. (Original) The method as in claim 2, wherein the carrier passivation layer is about 100 angstroms.

5. (Original) The method as in claim 2, wherein the membrane is less than one micron in thickness.

6. (Original) The method as in claim 2, wherein the membrane is silicon.

7. (Original) The method as in claim 2, wherein the membrane is made of a material other than silicon.

8. (Original) The method as in claim 1, further comprising:
forming a through hole through the device wafer to connect the surface of the device wafer and an opposing surface of the device wafer; and

bonding a back wafer to the opposing surface of the device wafer to cover the through hole.

9. (Original) The method as in claim 8, further comprising patterning the back wafer to have a sealing pattern around the through hole to seal the through hole.

10. (Original) The method as in claim 9, further comprising:

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after the removal of the carrier passivation layer, patterning the back wafer to expose the through hole through the back wafer.

Claims 11-19 (Cancelled).

20. (Original) A method, comprising:

preparing a carrier wafer to have a support wafer made of silicon, a carrier passivation layer formed on a surface of the support wafer, a membrane formed on the carrier passivation layer, and a plurality of posts on the membrane, wherein the carrier passivation layer is inert to a gaseous etchant that etches silicon;

placing the carrier wafer on a device wafer to bond the posts to the device wafer;

forming a passivation layer on exterior surfaces of the device wafer while leaving the support wafer exposed;

exposing the bonded carrier wafer and the device wafer to the gaseous etchant to etch away the support wafer in the carrier wafer and to expose the carrier passivation layer; and

removing the carrier passivation layer to transfer the membrane to the device wafer.

21. (Original) The method as in claim 20, wherein the posts are metals.

22. (Original) The methods as in claim 20, wherein the posts are silicon.

23. (Original) The method as in claim 20, wherein the membrane is a metal.

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23. (Original) The method as in claim 20, wherein the membrane is a polymer.

24. (Original) The method as in claim 20, wherein the membrane is a material different from silicon.